I claim:

1. A design verification system for verifying functionality of electronic designs, comprising:

at least one programmable logic device, said programmable logic device comprising a plurality of logic elements that can be placed in electrical communication with one another;

at least one logic processor programmed into said programmable logic device, said at least one logic processor utilizing at least one of said plurality of logic elements of said programmable logic device, said at least one logic processor comprising a logic functional unit that executes Boolean instructions;

at least one macro processor programmed into said programmable logic device, said at least one macro processor utilizing at least one of said plurality of logic elements of said programmable logic device, said at least one macro processor comprising a macro functional unit that executes macro instructions; and

an interconnect architecture programmed into said programmable logic device, said interconnect architecture placing each of said at least one logic processor and said at least one macro processor in communication with every other of said at least one logic processor and said at least one macro processor.

2. The design verification system of claim 1 further comprising at least one memory processor programmed into said programmable logic device, said at least one memory processor comprising a memory functional unit that can store data, said at least one memory processor in communication with said at least one logic processor and said at least one macro processor through said interconnect architecture.

3. The design verification system of claim 2 wherein said at least one memory processor comprises:

an instruction memory;

a register file controlled by said instruction memory, said register file having outputs selectively in communication said memory functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said memory functional unit.

4. The design verification system of claim 2 wherein said interconnect architecture comprises:

an instruction memory;

a plurality of buffers, wherein the number of said plurality buffers is equal to the sum of the number of said at least one logic processor added to the number of said at least one macro processor added to the number of said at least one memory processor, each of said plurality of buffers having an output that is selected by said instruction memory;

a plurality of selectors, wherein the number of said plurality of selectors is equal to the number of said plurality of buffers, each of said plurality of selectors in communication with each of said plurality of buffers so that data stored in any of said plurality of buffers can be transmitted to any of said plurality of selectors, each of said plurality of selectors controlled by said instruction memory; and

a plurality of output ports, each of said plurality of output ports corresponding to one of said plurality of selectors.

5. The design verification system of claim 1 further comprising a general purpose processor, said general purpose processor comprising a central processing unit that executes computer instructions, said general purpose processor in communication with said at least one logic processor and said at least one macro processor through said interconnect architecture.

6. The design verification system of claim 1 wherein said logic processor comprises:

an instruction memory;

a register file controlled by said instruction memory, said register file having outputs selectively in communication with said logic functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said logic functional unit.

7. The design verification system of claim 1 wherein said macro processor comprises:

an instruction memory; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication said macro functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said macro functional unit.

8. A method for implementing a design verification system into at least one programmable logic device so that a user design to be verified can be implemented therein, comprising:

mapping the user design into operations for execution;

partitioning each of said operations into processor types suitable for each of said operations;

ordering each of said processor types according to connectivity of each of said processor types;

scheduling communications between each of said processor types; and

programming each of said at least one programmable logic device with each of said processor types.

9. The method of claim 8 wherein said processor types comprise logic processors, macro processors, memory processors and general purpose processors.

10. The design verification system of claim 9 wherein said memory processor comprises;

an instruction memory;

a memory functional unit that can store data; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication said memory functional unit, said register file comprised of input registers and local registers, said local registers in communication with output from said memory functional unit.

11. The design verification system of claim 9 wherein said general purpose processor comprises a central processing unit that executes computer instructions.

12. The design verification system of claim 9 wherein said logic processors comprise:

an instruction memory;

a logic functional unit that executes Boolean logic instructions; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication with said logic functional unit, said register file comprised of input registers and local registers, said local registers in communication with output from said logic functional unit.

13. The design verification system of claim 9 wherein said macro processors comprise:

an instruction memory;

a macro processor executes macro instructions; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication said macro functional unit, said register file comprised of input registers and local registers, said local registers in communication with output from said macro functional unit.

14. The method of claim 8 wherein said partitioning step comprises:

consulting a programmable logic device library that has a preprogrammed mix of said processor types; and

selecting an appropriate preprogrammed mix of said processor types for said operations for execution.

15. The method of claim 8 wherein said scheduling step comprises:

creating a program for instruction memories within each of said processor types; and

creating programming files for each programmable logic device used for verifying the user design.

16. The method of claim 15 further comprising loading said program into each of said instruction memories.

17. A method for verifying functionality of an electronic design, the electronic design including Boolean logic gates, at least one macro function and at least one memory circuit, comprising;

compiling the electronic design into logic processors that execute the Boolean logic gates, at least one macro processor that executes the at least one macro function, at least one memory processor that executes the at least one memory circuit, and an interconnect architecture that interconnects said logic processors, said at least one macro processor and said at least one memory processor to one another;

programming said logic processors, said at least one macro processor and said at least one memory processor into at least one programmable logic device;

applying stimulus to said logic processors programmed into said at least one programmable logic device, said at least one macro processor programmed into said at least one programmable logic device and said at least one memory processor programmed into said at least one programmable logic device such that said logic processors execute the Boolean logic gates,

said at least one macro processor executes the at least one macro function and said at least one memory processor executes the at least one memory circuit; and

collecting output responses generated by said logic processors programmed into said at least one programmable logic device, said at least one macro processor programmed into said at least one programmable logic device and said at least one memory processor programmed into said at least one programmable logic device.

18. The design verification system of claim 17 wherein said interconnect architecture further comprises:

an instruction memory;

a plurality of buffers, wherein the number of said plurality buffers is equal to the sum of the number of said logic processors added to the number of said at least one macro processor added to the number of at least one said memory processor, each of said plurality of buffers having an output that is selected by said instruction memory;

a plurality of selectors, wherein the number of said plurality of selectors is equal to the number of said plurality of buffers, each of said plurality of selectors in communication with each of said plurality of buffers so that data stored in any of said plurality of buffers can be transmitted to any of said plurality of selectors, each of said plurality of selectors controlled by said instruction memory; and

a plurality of output ports, each of said plurality of output ports corresponding to one of said plurality of selectors.

19. The design verification system of claim 17 wherein said at least one memory processor comprises:

an instruction memory;

a register file controlled by said instruction memory, said register file having outputs selectively in communication said memory functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said memory functional unit.

20. The design verification system of claim 17 further comprising a general purpose processor, said general purpose processor comprising a central processing unit that executes computer instructions, said general purpose processor in communication with said logic processors and said at least one macro processor through said interconnect architecture.

21. The design verification system of claim 17 wherein said logic processors comprise:

an instruction memory;

a register file controlled by said instruction memory, said register file having outputs selectively in communication said logic functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said logic functional unit.

22. The design verification system of claim 17 wherein said at least one macro processor comprises:

an instruction memory; and

a register file controlled by said instruction memory, said register file having outputs selectively in communication said macro functional unit, said register file comprised of input registers and local registers, said input registers in communication with said interconnect architecture, said local registers in communication with output from said macro functional unit.